

LIST OF REFERENCES CITED BY  
APPLICANT & TRADEMARK OFFICE  
(use as many sheets as necessary)

Application Number: 09/911,038  
 Filing Date: July 23, 2001  
 First Named Inventor: Eiji OKI  
 Group Art Unit: Not yet assigned  
 Examiner Name: Not yet assigned

Sheet 1 of 1 Attorney Docket No.: Poly-22-2/APP

## OTHER REFERENCES - NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume, issue number(s), publisher, country, where published, source	T <sup>2</sup>
JH	AA.	N. W. McKeown, "Scheduling Algorithms for Input-Queued Cell Switches," PhD Thesis, University of California at Berkeley, (1995).	
JH	AB.	C. Y. Lee and A. Y. Oruç, "A Fast Parallel Algorithm for Routing Unicast Assignments in Benes Networks," <u>IEEE Trans. on Parallel and Distributed Sys.</u> , Vol. 6, No. 3, pp. 329-334 (March 1995).	
JH	AC.	T. T. Lee and S-Y Liew, "Parallel Routing Algorithms in Benes-Clos Networks," <u>Proc. IEEE INFOCOM '96</u> , pp. 279-286 (1996).	
JH	AD.	N. McKeown, M. Izzard, A. Mekittikul, W. Ellersick and M. Horowitz, "Tiny-Tera: A Packet Switch Core," <u>IEEE Micro.</u> , pp. 26-33 (Jan-Feb. 1997).	
JH	AE.	T. Chaney, J. A. Fingerhut, M. Flucke, J. S. Turner, "Design of a Gigabit ATM Switch," <u>Proc. IEEE INFOCOM '97</u> , pp. 2-11 (April 1997).	
JH	AF.	F. M. Chiussi, J. G. Kneuer, and V. P. Kumar, "Low-Cost Scalable Switching Solutions for Broadband Networking: The ATLANTA Architecture and Chipset," <u>IEEE Commun. Mag.</u> , pp. 44-53 (Dec. 1997).	
JH	AG.	J. Turner and N. Yamanaka, "Architectural Choices in Large Scale ATM Switches," <u>IEICE Trans. Commun.</u> , Vol. E81-B, No. 2, pp. 120-137 (Feb. 1998).	
JH	AH.	H. J. Chao and J-S Park, "Centralized Contention Resolution Schemes for a Large-Capacity Optical ATM Switch," <u>Proc. IEEE ATM Workshop '97</u> , pp. 11-16 (Fairfax, VA, May 1998).	
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JH	AJ.	N. McKeown, "The iSLIP Scheduling Algorithm for Input-Queued Switches," <u>IEEE/ACM Transactions on Networking</u> , Vol. 7, No. 2, pp. 188-201 (April 1999).	
JH	AK.	A. Smiljanić, R. Fan and G. Ramamurthy, "RRGS-Round-Robin Greedy Scheduling for Electronic/Optical Terabit Switches," <u>Global Telecommunications Conference - Globecom '99</u> , pp. 1244-1250 (May 1999).	
JH	AL.	N. McKeown, A. Mekittikul, V. Anantharam, and J. Walrand, "Achieving 100% Throughput in an Input-Queued Switch," <u>IEEE Trans. on Communications</u> , Vol. 47, No. 8, pp. 1260-1267 (Aug. 1999).	
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JH	AN.	N. Yamanaka, E. Oki, S. Yasukawa, R. Kawano and K. Okazaki, "OPTIMA: Scalable, Multi-Stage, 640-Gbit/s ATM Switching System Based on Advanced Electronic and Optical WDM Technologies," <u>IEICE Trans. Commun.</u> , Vol. E83-B, No. 7, pp. 1488-1496 (July 2000).	
JH	AO.	J. Chao, "Saturn: A Terabit Packet Switch Using Dual Round-Robin," <u>IEEE Communications Magazine</u> , pp. 78-84 (Dec. 2000).	
JH	AP.	G. Nong and M. Hamdi, "On the Provision of Quality-of-Service Guarantees for Input	

HH		Queued Switches," IEEE Commun. Mag., pp. 62-69 (Dec. 2000).	
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HH	AS.	A. Smiljanić, "Flexible Bandwidth Allocation in Terabit Packet Switches," pp. 233-239.	

Examiner Signature		Date Considered	08/01/2005
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Unique citation designation number. 2 Applicant is to place a check mark here if English language translation is attached.

